REMARKS

Claims 1-30 are pending in the application.

The title is objected to as allegedly not being descriptive.

The drawings are objected to as allegedly not showing every feature of the invention as specified in the claims.

Claims 10-26 are objected to for informalities.

Claims 1-30 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-30 of copending Application No. 09/572,047.

Claims 1-6, 9, and 27-29 stand rejected under 35 U.S.C. 102(e) as allegedly being anticipated by U.S. Patent Number 6,167,487 to Comacho et al. ("Comacho").

Claims 1-6, 9, and 27-29 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent Number 5,852,608 to Csoppenszky et al. ("Csoppenszky").

Claims 1-6, 9, and 27-29 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent Number 4,371,932 to Dinwiddle, Jr. et al. ("Dinwiddie").

Claims 7 and 30 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Camacho, Csoppenszky, or

Dinwiddie, in view of U.S. Patent Number 5,784,699 to McMahon et al. ("McMahon").

Claim 8 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Camacho, Csoppenszky, or Dinwiddie, in view of U.S. Patent Number 5,546,554 to Yung et al. ("Yung").

Claims 10-26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Dinwiddie or U.S. Patent Number 6,167,487 to Chin et al. ("Chin"), in view of McMahon.

Applicant respectfully traverses the rejections in view of the amendments and following remarks.

I. The Title

Applicant has amended the title to read "Accessing multi-ported memory for uncached status and control accesses."

II. The Drawings

Applicant has added figure 4, showing process steps for an embodiment of the invention. No new matter is added (see, e.g., originally filed claims 10, 14, 19, and 23).

III. The Informalities

Applicant believes that the claim amendments have corrected all informalities noted in the office action.

IV. The provisional double patenting rejection

Applicant acknowledges the provisional double patenting rejection of claims 1-30, and will make any necessary claim amendments and/or cancellations at such time as claims are allowed in one of the applications.

V. The Rejections under 35 U.S.C. 102

Claims 1-6, 9, and 27-29 stand rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Comacho, and stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Csoppenszky or Dinwiddie.

Claim 1

Claim 1 is patentable over Comacho, Csoppenszky, and Dinwiddie, because none of the references teach or suggest a computer system "wherein the computer system is configured so that control accesses from the central processing unit are directed to the multi-ported memory and data accesses from the central processing unit are directed to the main memory," as recited in claim 1.

Comacho

Applicant finds no teaching or suggestion in Comacho that data accesses from the CPU be directed to a main memory and

control accesses from the CPU be directed to a multi-ported memory. Instead, Comacho teaches a multi-port RAM having interchangeable input/output ports, which allows read and write accesses from different ports to be performed simultaneously, where the multi-port RAM would be fully functional through one port if the other port is disabled, and where the multi-port RAM can combine its two input/output ports into a single input/output port twice as wide as each port of the RAM. (See, e.g., column 1, line 62 to column 2, line 9 of Comacho).

A computer system according to claim 1 provides a number of advantages not found in Comacho. First, by directing control accesses to the multi-ported memory rather than a main memory, a bus snoop and its attendant delay are avoided. (See, e.g. page 4, lines 3-8 of the specification, discussing an exemplary embodiment). Second, increased usage of the multi-ported memory for control accesses reduces the use of the main memory, and allows for less data traffic on the associated data channel. With less traffic, the CPU may be able to transfer more data to/from the main memory in a given time. (See, e.g., page 7, line 22 to page 8, line 4 of the specification, discussing an exemplary embodiment).

At least because Comacho does not teach or suggest that data accesses from the CPU be directed to a main memory and

control accesses from the CPU be directed to a multi-ported memory, claim 1 is patentable over Comacho.

Csoppenszky

Applicant finds no teaching or suggestion in Csoppenszky that data accesses from the CPU be directed to a main memory and control accesses from the CPU be directed to a multi-ported memory. Instead, Csoppenszky teaches a method and structure for operably coupling two systems having asynchronous clock domains in an area efficient manner, that operates with a bi-directional manner with low standby power and a high data rate. (See, e.g., column 1, lines 54-59 of Csoppenszky).

By providing a computer system where data accesses from the CPU are directed to the main memory while control accesses from the CPU are directed to the main memory, a computer system according to claim 1 provides a number of advantages not found in Csoppenszky (see the section dealing with the Comacho reference, above). At least because Csoppenszky does not teach or suggest this feature of claim 1, claim 1 is patentable over Csoppenszky.

Dinwiddie

Applicant finds no teaching or suggestion in Dinwiddie that data accesses from the CPU be directed to a main memory and control accesses from the CPU be directed to a multi-ported

memory. Instead, Dinwiddie is directed to an input/output controller for use in digital data processing systems for transferring data between a host processor and one or more peripheral units or I/O units. (See, e.g., column 1, lines 32-35 of Dinwiddie.

By providing a computer system where data accesses from the CPU are directed to the main memory while control accesses from the CPU are directed to the multi-ported memory, a computer system according to claim 1 provides a number of advantages not found in Dinwiddie (see the section dealing with the Comacho reference, above). At least because Dinwiddie does not teach or suggest this feature of claim 1, claim 1 is patentable over Dinwiddie.

Claims 2-8

Claims 2-8 depend from claim 1 and are therefore patentable for at lest the same reasons as stated above with respect to claim 1.

Claim 27

Claim 27 stands rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Comacho, and under 35 U.S.C. 102(b) as allegedly being anticipated by Csoppenszky and Dinwiddie.

As amended, claim 27 recites an integrated circuit including a CPU, multi-ported memory, and main memory, "wherein control accesses for the CPU are directed to the multi-ported memory and wherein data accesses for the CPU are directed to the main memory."

Therefore, for the same reasons as stated above with respect to claim 1, claim 27 is patentable over Comacho, Csoppensky, and Dinwiddie.

Claims 28-29

Claims 28-29 depend from claim 27 and are therefore patentable for at least the same reasons as stated above with respect to claim 27.

V. The Rejections under 35 U.S.C. 103

Claim 10

Claim 10 stands rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Dinwiddie or Chin, in view of McMahon.

However, neither Dinwiddie, Chin, nor McMahon teach or suggest "routing a data access from a peripheral device to a first memory in the computer; and routing a status access from a peripheral device to a second memory in the computer," as recited in claim 10.

Specifically, none of the references teach or suggest "routing a status access from a peripheral device to a second memory in the computer," as recited in claim 10. The office action cites Figure 1 of McMahon as disclosing "making from a peripheral device, a status access to memory in the computer and routing the status access to a second memory in the computer (Fig 1) for the purpose of providing fast search and allocation/deallocation of availability of a memory block." (See page 12, paragraph 18 of the office action).

Applicant disagrees. According to McMahon, Figure 1 of McMahon is "a block diagram illustrating one embodiment for a software system that incorporates the dynamic memory allocator of the present invention." (See column 4, lines 58-60 of McMahon). "In operation, the dynamic memory allocator 50 receives memory requests from software programs 20. A memory request includes a size that specifies the amount of memory required. In response, the dynamic memory allocator 50 returns a pointer to a memory block that fulfills the memory request." (See column 4, line 65 to column 5, line 3 of McMahon). That is, the dynamic memory allocator of Figure 1 chooses a memory block within a memory that fulfills the memory request (i.e. is large enough to accommodate the request). This is entirely different than routing a data access to a first memory and a

control/status access to a second memory. In fact, Applicant finds no indication in Figure 1 (or elsewhere in McMahon) that data accesses are treated at all differently from control/status accesses.

At least because McMahon does not teach or suggest "routing a status access from a peripheral device to a second memory in the computer," as recited in claim 10, the combination of McMahon with either Dinwiddie or Chin does not include all elements of claim 10. Therefore, claim 10 is patentable over Dinwiddie, Chin, and McMahon, alone or in combination.

Claims 11-13

Claims 11-13 depend from claim 10, and are therefore patentable for at least the same reasons as stated above with respect to claim 10.

Claim 14

Claim 14 recites "an article comprising a computer-readable medium which stores computer-executable instructions for memory accessing, the instructions causing a machine to: route a data access from a peripheral device to a first memory in the computer; and route a status access from the peripheral device to a second memory in the computer." For at least the same reasons as stated above with respect to claim 10, claim 14 is

patentable over Dinwiddie, Chin, and McMahon, alone or in combination.

Claims 15-18

Claims 15-18 depend from claim 14 and are therefore patentable for at least the same reasons as stated above with respect to claim 14.

Claim 19

Claim 19 recites "routing the a data access from a central processing unit to a first memory in the computer; and routing a control access from the central processing unit to a second memory in the computer."

Again, the office action contends that "McMahon discloses making from the CPU, a status access to memory in the computer and routing the status access to a second memory in the computer (Fig. 1) for the purpose of providing fast search and allocation/deallocation of availability of a memory block." (See page 14 of the office action). As stated above with respect to claim 10, McMahon does not so teach.

At least because none of the cited references teach or suggest this feature of claim 19, claim 19 is patentable over Dinwiddie, Chin, and McMahon, alone or in combination.

Claims 20-22

Claims 20-22 depend from claim 19, and are therefore patentable for at least the same reasons as stated above with respect to claim 19.

Claim 23

Claim 23 recites "An article comprising a computer-readable medium which stores computer-executable instructions for memory accessing, the instructions causing a machine to: route a data access from a central processing unit to a first memory in the computer; and route a control access from the central processing unit to a second memory in the computer."

For at least the same reasons as stated above with respect to claim 19, claim 23 is patentable over Dinwiddie, Chin, and McMahon, alone or in combination.

Claims 24-26

Claims 24-26 depend from claim 23, and are therefore patentable for at least the same reasons as stated above with respect to claim 23.

Attached is a marked-up version of the changes being made by the current amendment.

CONCLUSION

For at least the foregoing reasons, Applicant believes that claims 1-8 and 10-33 are in condition for allowance. Applicant asks that all claims be allowed.

Enclosed is a $36 check for excess claim fees. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 8/23/02

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Version with markings to show changes made

In the title:

Accessing multi-ported memory for uncached status and control accesses

In the claims:

Claim 9 has been cancelled.

Claims 1, 6, 10, 14, 18, 19, 21, 23, 27, and 29 have been amended as follows:

1. (Amended) A computer system, comprising:

a non-cached multi-ported memory;

a main memory;

a central processing unit coupled to the multi-ported memory;

[a peripheral device] a bus configured to communicate with one or more peripheral devices, the bus coupled to the multi-ported memory and configured to access the multi-ported memory independently of the central processing unit;

wherein the computer system is configured so that control accesses from the central processing unit are directed to the multi-ported memory and data accesses from the central processing unit are directed to the main memory[the central

processing unit and the peripheral device being configured to access the multi-ported memory independently].

6. (Amended) The system of claim 1, wherein the multi-ported memory is chosen from the group consisting of static random access memory [or] and dynamic random access memory.

10. (Amended) A method comprising:

[making, from a peripheral device, a data access to a memory in a computer;

making, from the peripheral device, a status access to a memory in the computer;]

routing [the] a data access from a peripheral device to a first memory in the computer; and

routing [the] a status access from a peripheral device to a second memory in the computer.

14. (Amended) An article comprising a computer-readable medium which stores computer-executable instructions for memory accessing, the instructions causing a machine to:

[make, from a peripheral device, a data access to memory in a computer;

make, from the peripheral device, a status access to memory in the computer;]

route [the] a data access from a peripheral device to a first memory in the computer; and

route [the] a status access from the peripheral device to a second memory in the computer.

18. (Amended) The [product] article of claim 14, wherein the second memory is dual-ported.

19. (Amended) A method comprising:

[making, from a central processing unit, a data access to memory in a computer;

making, from a peripheral device, a control access to memory in the computer;]

routing the a data access from a central processing unit to a first memory in the computer; and

routing [the] a control access from the central processing unit to a second memory in the computer.

21. (Amended) The method of claim 19, wherein the second memory [comprises memory] is included in a memory controller.

23. (Amended) An article comprising a computer-readable medium which stores computer-executable instructions for memory accessing, the instructions causing a machine to:

[make, from a central processing unit, a data access to memory in a computer;

make, from the central processing unit, a control access to memory in the computer;]

route [the] a data access from a central processing unit to a first memory in the computer; and

route [the] a control access from the central processing unit to a second memory in the computer.

27. (Amended) An integrated circuit comprising:

a memory controller configured to communicate with a CPU, a peripheral device, and a main memory[including at least two electrical ports for coupling to communication channels; and], the memory controller including a multi-ported memory, wherein control accesses for the CPU are directed to the multi-ported memory and wherein data accesses for the CPU are directed to the main memory.

[multi-ported memory communicatively coupled to each port.]

29. (Amended) The integrated circuit of claim 27, wherein the multi-ported memory is chosen from the group consisting of static random access memory [or] and dynamic random access memory.